Fig. 1

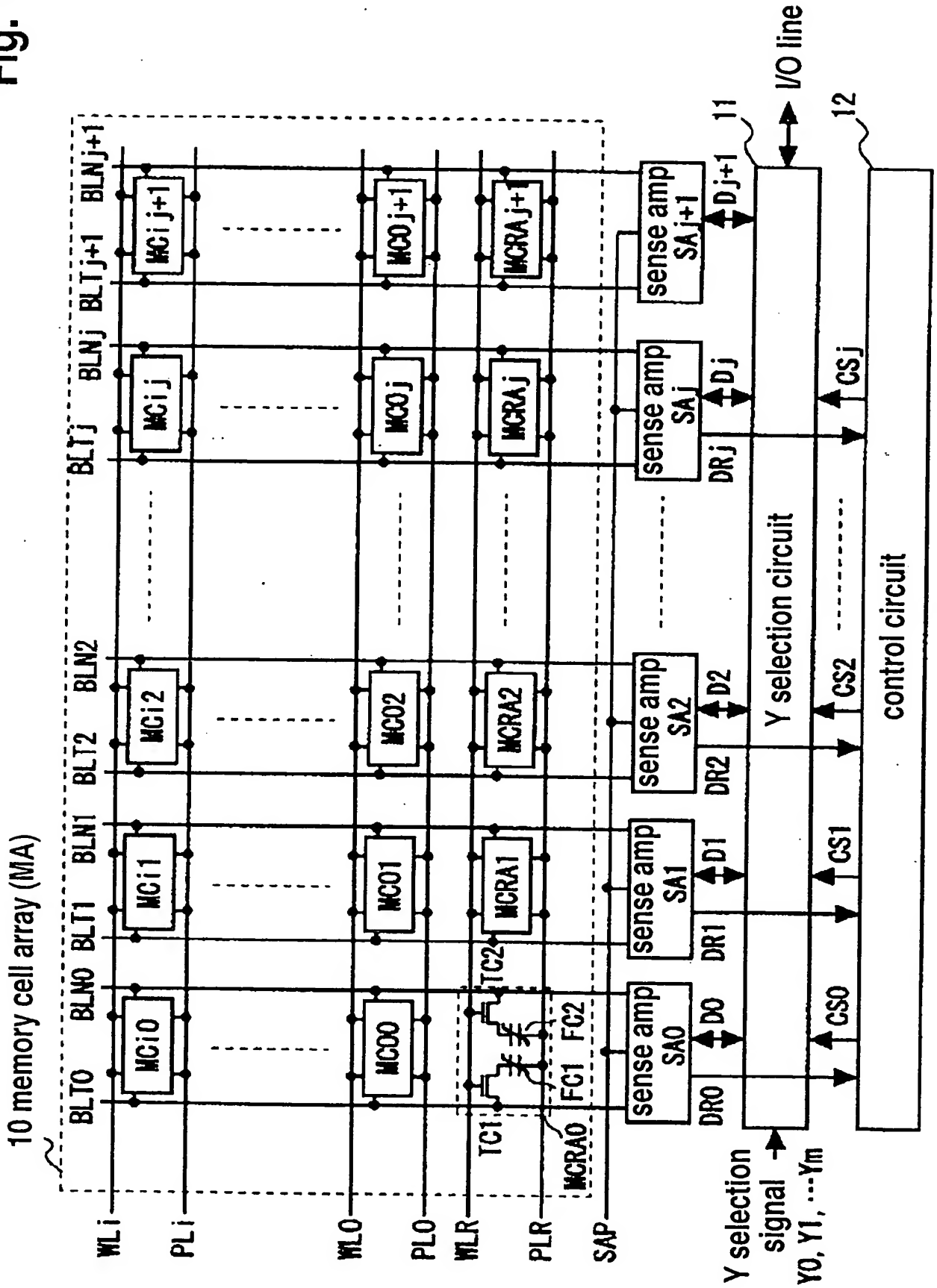

10 memory cell array (MA)
BLT0
BLN0
BLT1
BLN1
BLT2
BLN2
BLTj
BLNj
BLTj+1
BLNj+1
MCi0
MCi1
MCi2
MCij
MCij+1
MCO0
MCO1
MCO2
MCOj
MCOj+1
MCRA0
MCRA1
MCRA2
MCRAj
MCRAj+1
TC1
TC2
FC1
FC2
WLi
PLi
WL0
PL0
WLR
PLR
SAP
sense amp SA0
sense amp SA1
sense amp SA2
sense amp SAj
sense amp SAj+1
DR0
DR1
DR2
DRj
D0
D1
D2
Dj
Dj+1
11
I/O line
12
Y selection circuit
control circuit
CS0
CS1
CS2
CSj
Y selection signal
Y0, Y1, ···Ym

Fig. 2

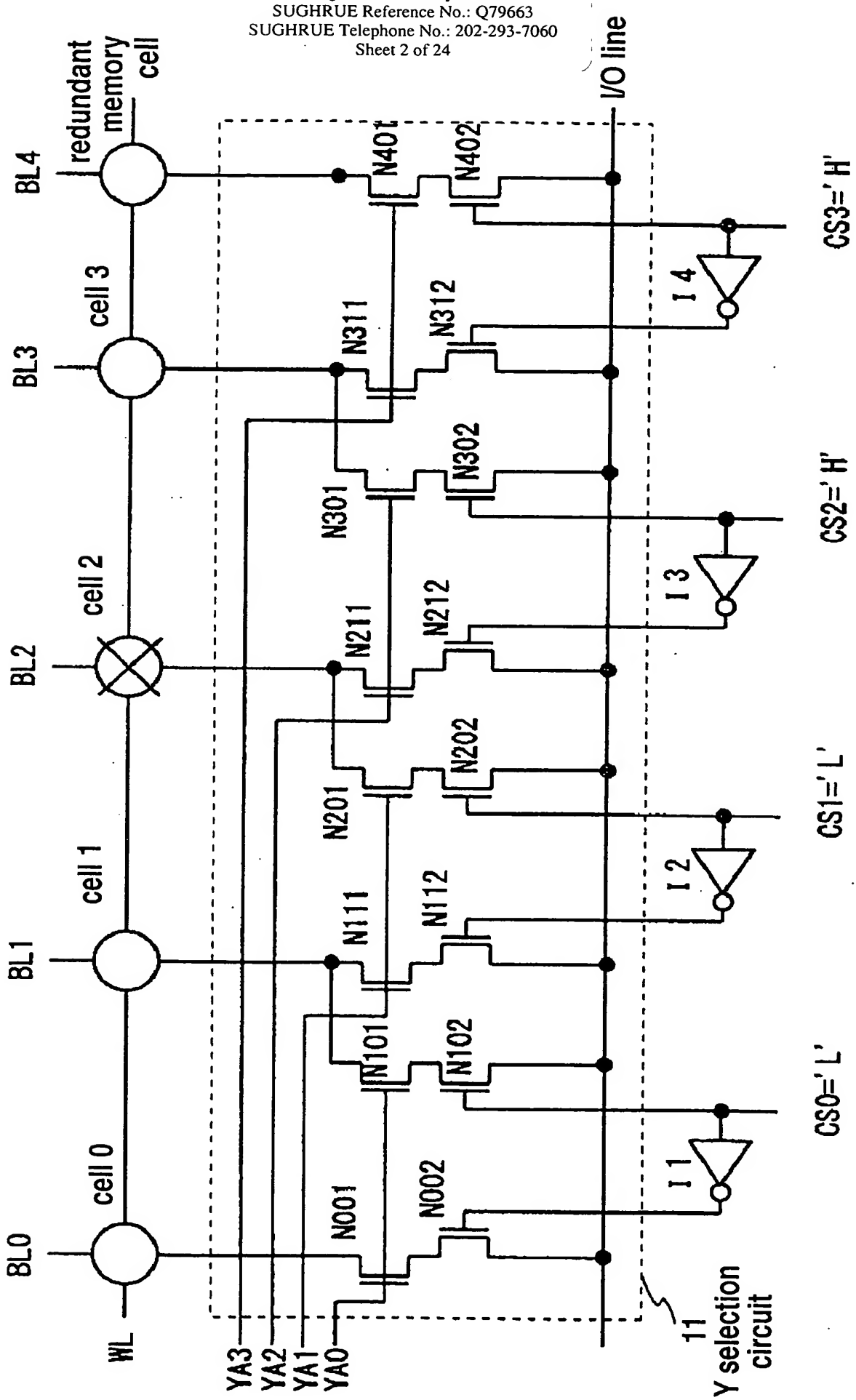

redundant memory cell
I/O line
BL4
BL3
BL2
BL1
BL0
cell 3
cell 2
cell 1
cell 0
WL
YA3
YA2
YA1
YA0
N401
N402
N311
N312
N301
N302
N211
N212
N201
N202
N111
N112
N101
N102
N001
N002
I 4
I 3
I 2
I 1
CS3='H'
CS2='H'
CS1='L'
CS0='L'
11
Y selection circuit

Fig. 3

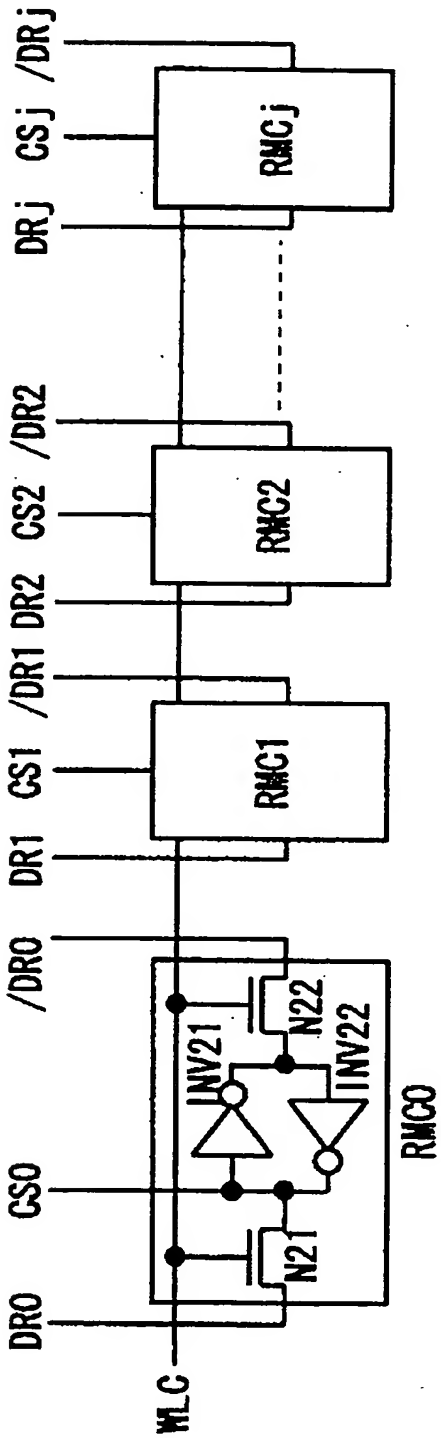

/DRj
CSj
DRj
RMCj
/DR2
CS2
DR2
RMC2
/DR1
CS1
DR1
RMC1
/DR0
CS0
DR0
INV21
N22
INV22
N21
RMC0
WLC

Fig. 4

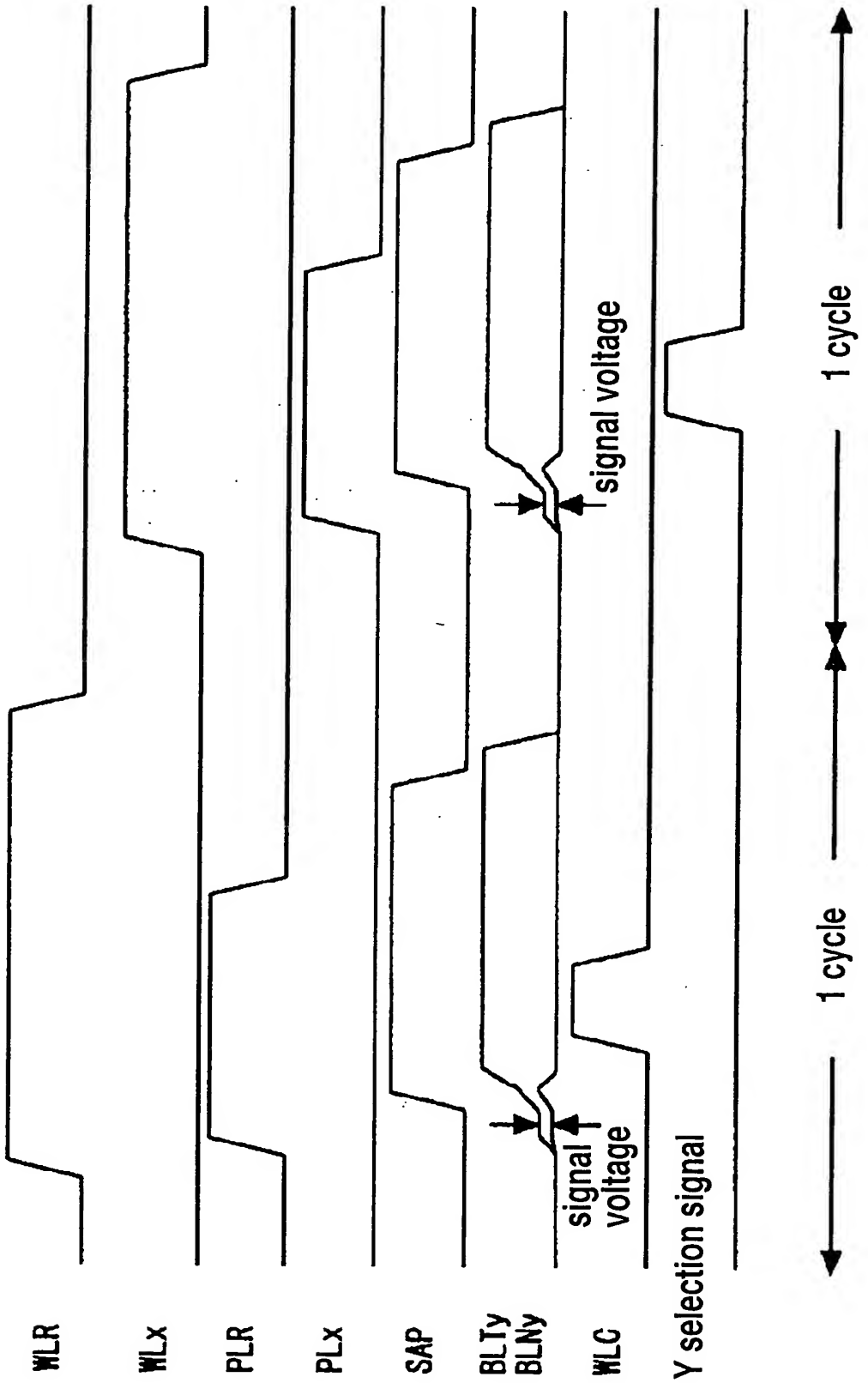

WLR
WLx
PLR
PLx
SAP
BLTy
BLNy
WLC
Y selection signal
signal voltage
signal voltage
1 cycle
1 cycle

Fig. 5

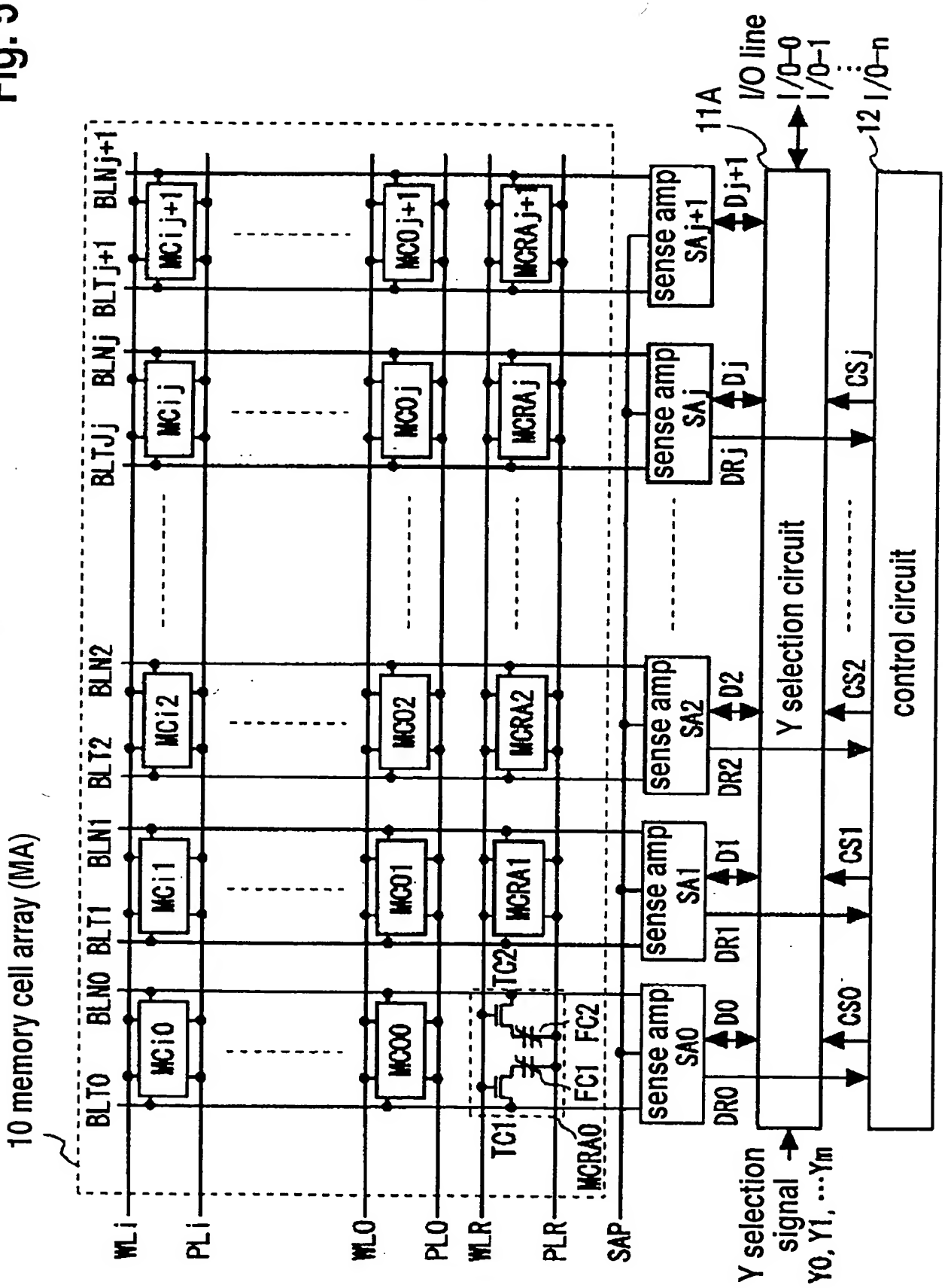

10 memory cell array (MA)
BLTO
BLNO
BLT1
BLN1
BLT2
BLN2
BLTJ
BLNJ
BLTj+1
BLNj+1
MCi0
MCi1
MCi2
MCij
MCij+1
MCO0
MCO1
MCO2
MCOj
MCOj+1
MCRA0
MCRA1
MCRA2
MCRAj
MCRAj+1
TC1
TC2
FC1
FC2
WLi
PLi
WLO
PLO
WLR
PLR
SAP
sense amp SA0
sense amp SA1
sense amp SA2
sense amp SAj
sense amp SAj+1
DR0
DR1
DR2
DRj
D0
D1
D2
Dj
Dj+1
11A
I/O line
I/O-0
I/O-1
I/O-n
12
Y selection circuit
control circuit
CS0
CS1
CS2
CSj
Y selection signal
Y0, Y1, ···Ym

Fig. 6

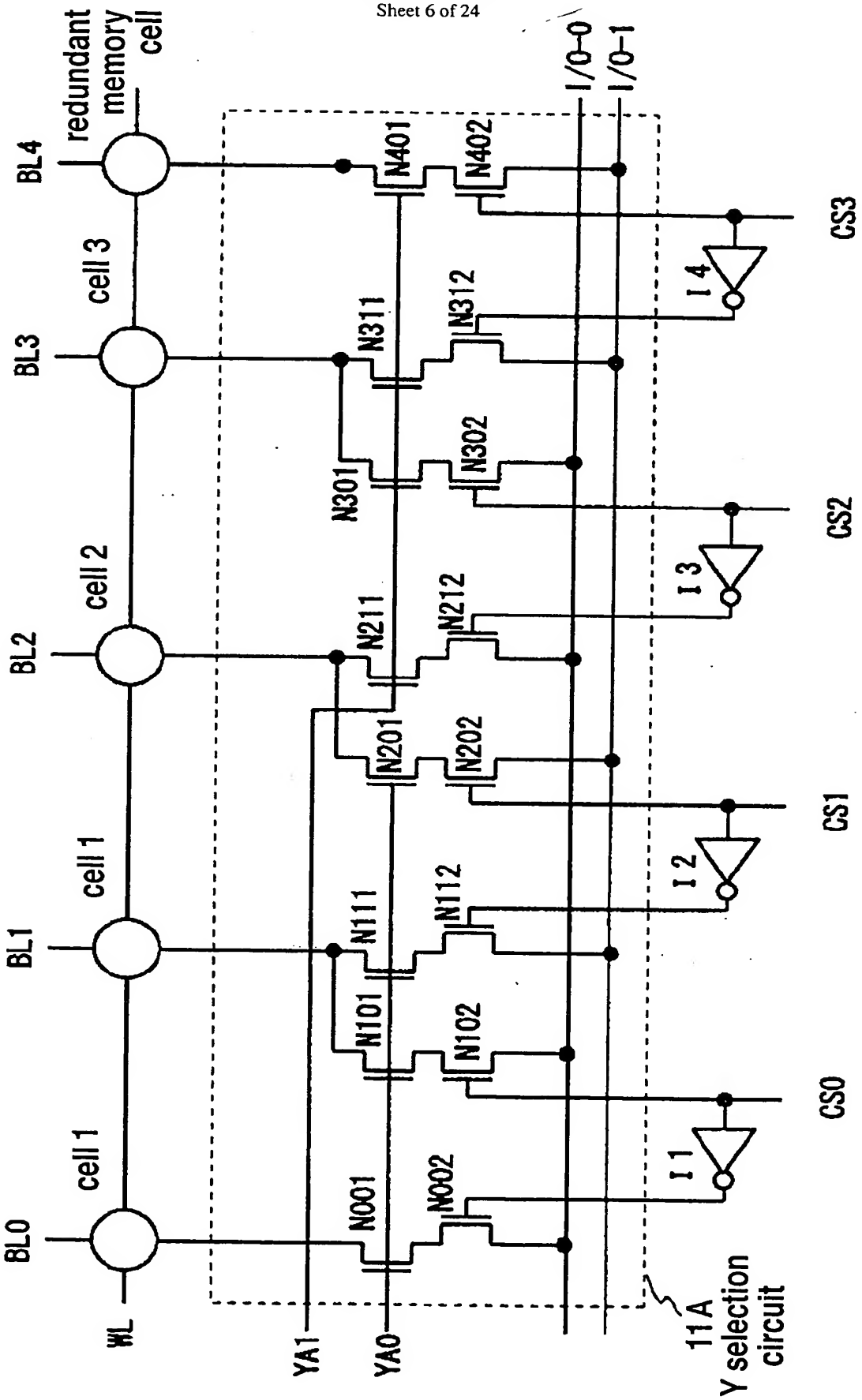

redundant memory cell
BL4
cell 3
BL3
cell 2
BL2
cell 1
BL1
cell 1
BL0
WL
YA1
YA0
I/O-0
I/O-1
N401
N402
N311
N312
N301
N302
N211
N212
N201
N202
N111
N112
N101
N102
N001
N002
I4
I3
I2
I1
CS3
CS2
CS1
CS0
11A
Y selection circuit

Fig. 7

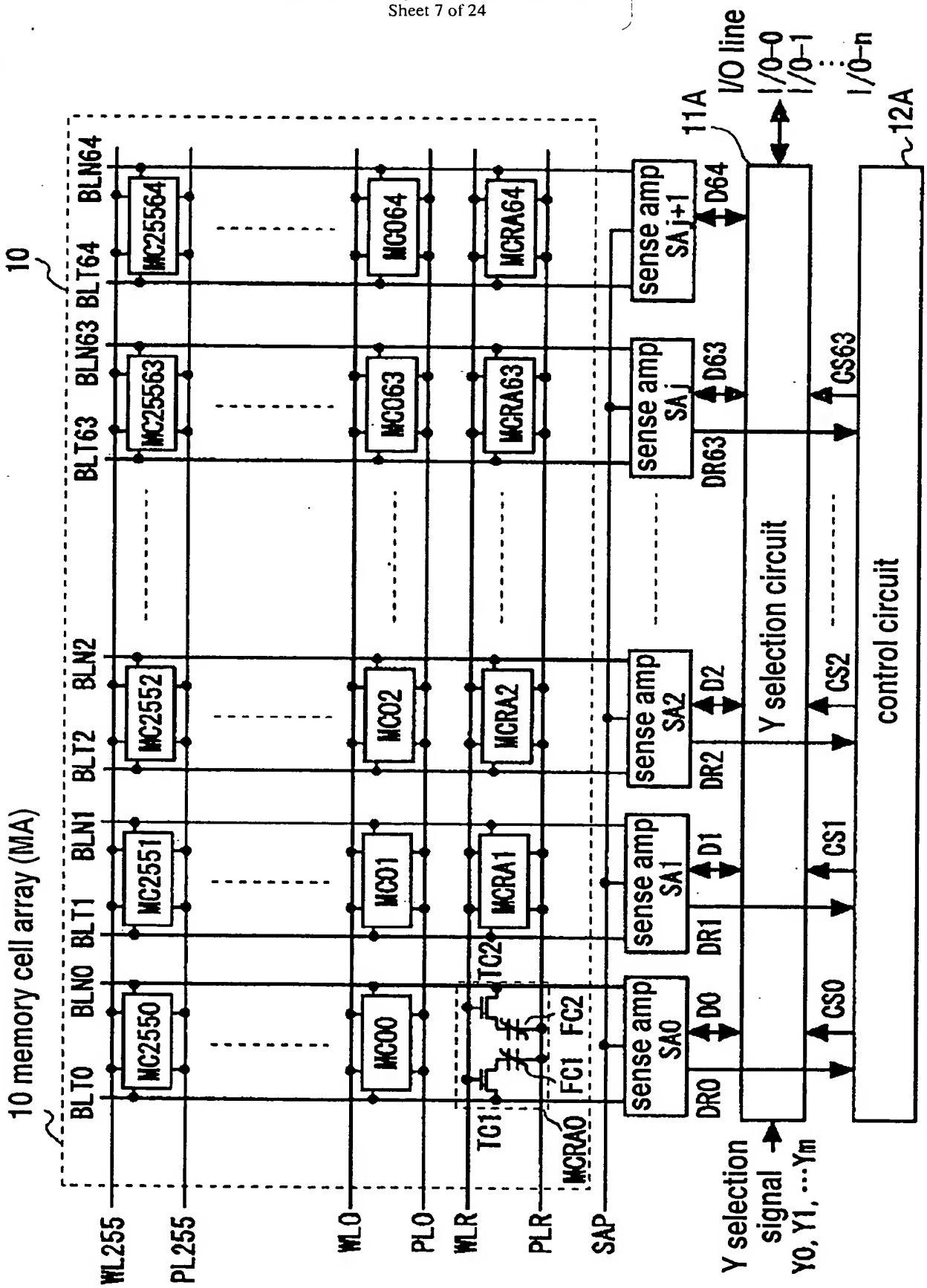

10
10 memory cell array (MA)
BLT0
BLN0
BLT1
BLN1
BLT2
BLN2
BLT63
BLN63
BLT64
BLN64
MC2550
MC2551
MC2552
MC25563
MC25564
MC00
MC01
MC02
MC063
MC064
MCRA0
MCRA1
MCRA2
MCRA63
MCRA64
TC1
TC2
FC1
FC2
WL255
PL255
WL0
PL0
WLR
PLR
SAP
sense amp SA0
sense amp SA1
sense amp SA2
sense amp SAj
sense amp SAj+1
D0
D1
D2
D63
D64
DR0
DR1
DR2
DR63
11A
Y selection circuit
CS0
CS1
CS2
CS63
I/O line
I/O-0
I/O-1
I/O-n
12A
control circuit
Y selection signal
Y0, Y1, ···Ym

Fig. 8

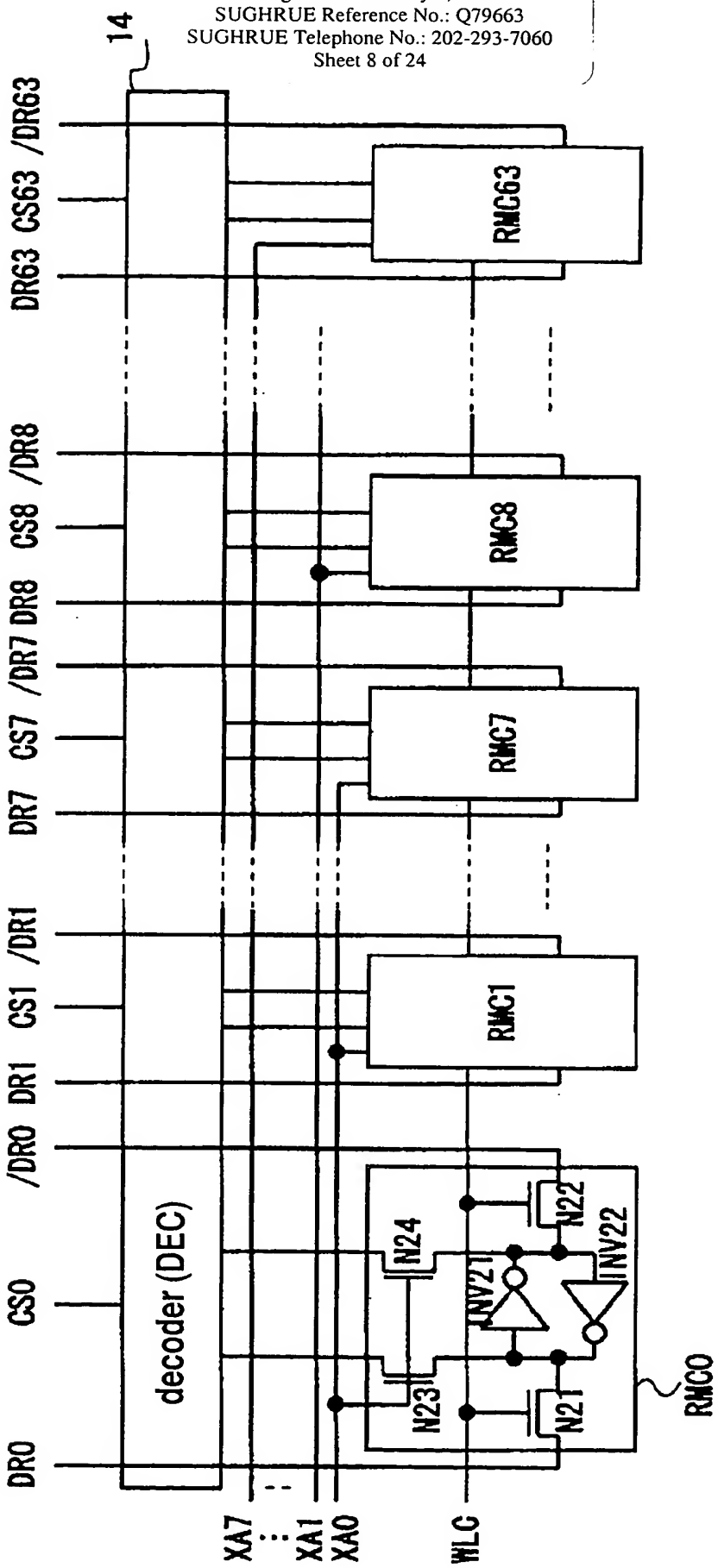

14
DR63
CS63
/DR63
DR8
CS8
/DR8
DR7
CS7
/DR7
DR1
CS1
/DR1
DR0
CS0
/DR0
RMC63
RMC8
RMC7
RMC1
RMC0
decoder (DEC)
N24
N23
N22
N21
INV21
INV22
XA7
XA1
XA0
WLC

Fig. 9

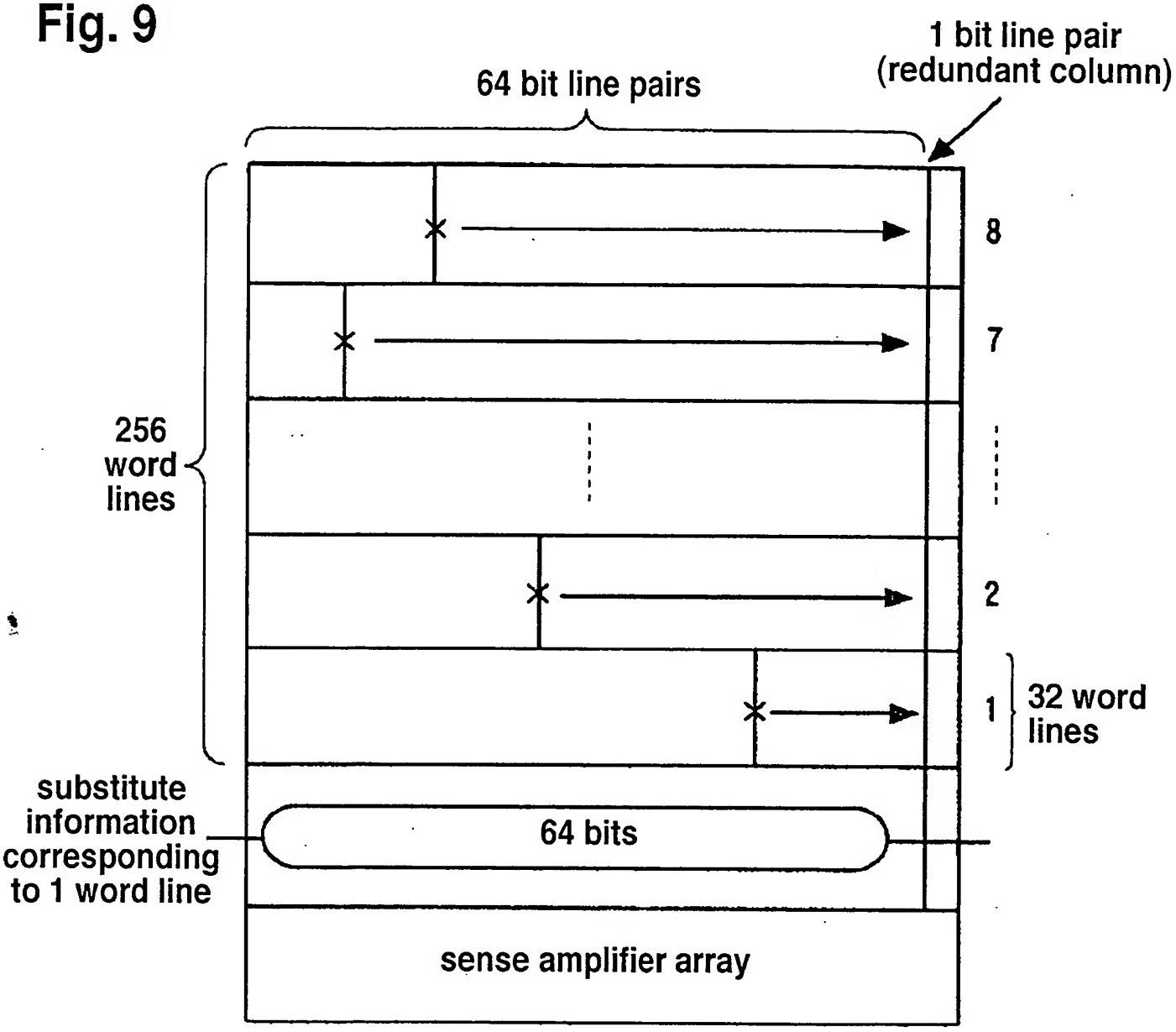

64 bit line pairs
1 bit line pair
(redundant column)
256
word
lines
8
7
2
1
32 word
lines
substitute
information
corresponding
to 1 word line
64 bits
sense amplifier array

Fig. 10

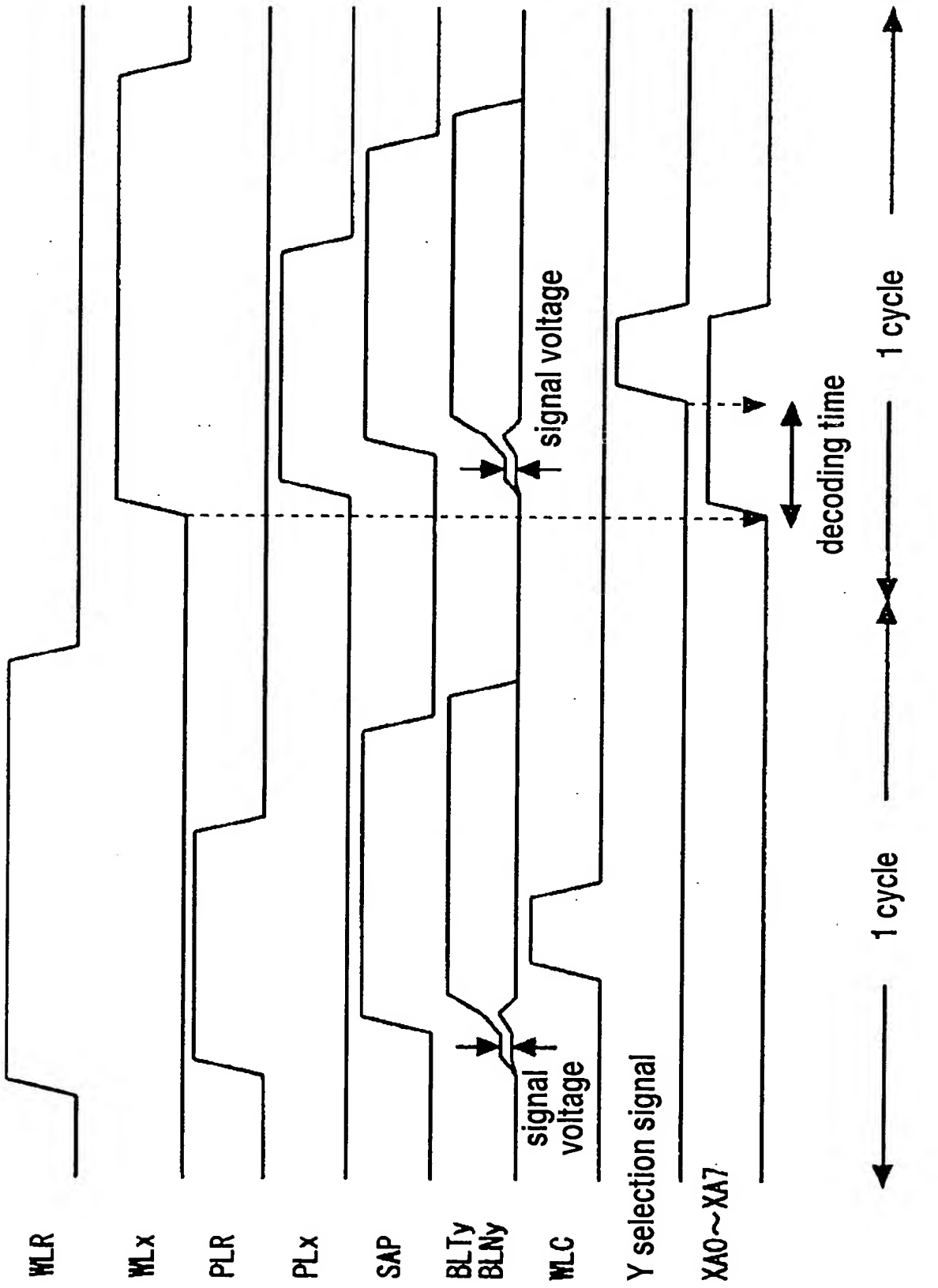

WLR
WLx
PLR
PLx
SAP
BLTy
BLNy
WLC
Y selection signal
XA0~XA7
signal voltage
signal voltage
decoding time
1 cycle
1 cycle

Fig. 11

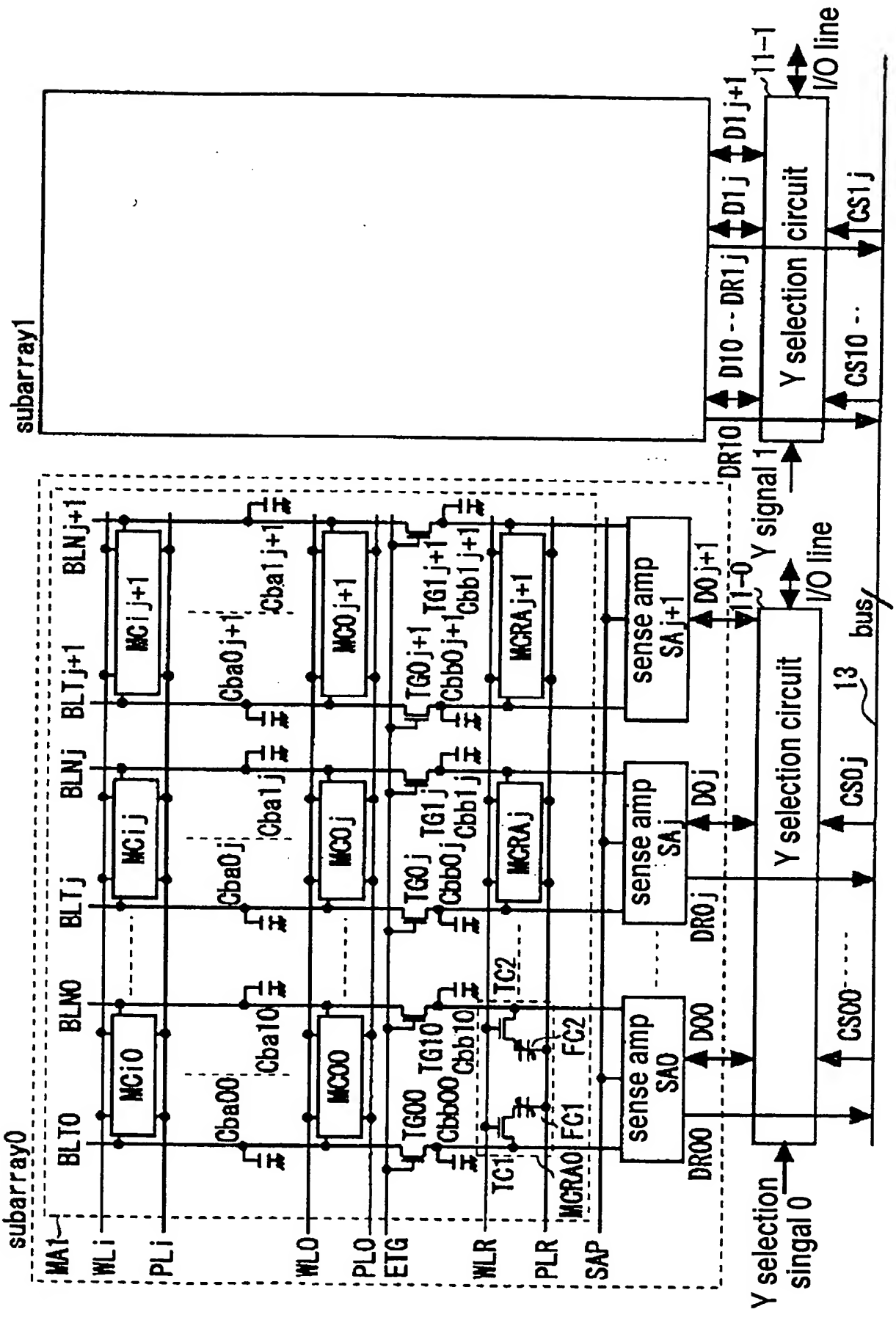

subarray1
subarray0
MA1
WLi
PLi
WLO
PLO
ETG
WLR
PLR
SAP
BLTO
BLNO
BLTj
BLNj
BLTj+1
BLNj+1
MCi0
MCOO
MCij
MCOj
MCij+1
MCOj+1
MCRA0
MCRAj
MCRAj+1
CbaOO
Cba10
CbaOj
Cba1j
CbaOj+1
Cba1j+1
TGOO
TG10
TGOj
TG1j
TGOj+1
TG1j+1
CbbOO
Cbb10
CbbOj
Cbb1j
CbbOj+1
Cbb1j+1
TC1
TC2
FC1
FC2
sense amp SA0
sense amp SAj
sense amp SAj+1
DRO0
DROj
DOO
DOj
DOj+1
Y selection singal 0
Y selection circuit
Y signal 1
I/O line
bus
13
11-0
11-1
CSOO
CSOj
DR10
D10 - - DR1j
D1j
D1j+1
CS10 - -
CS1j
Y selection circuit
I/O line

Fig. 12

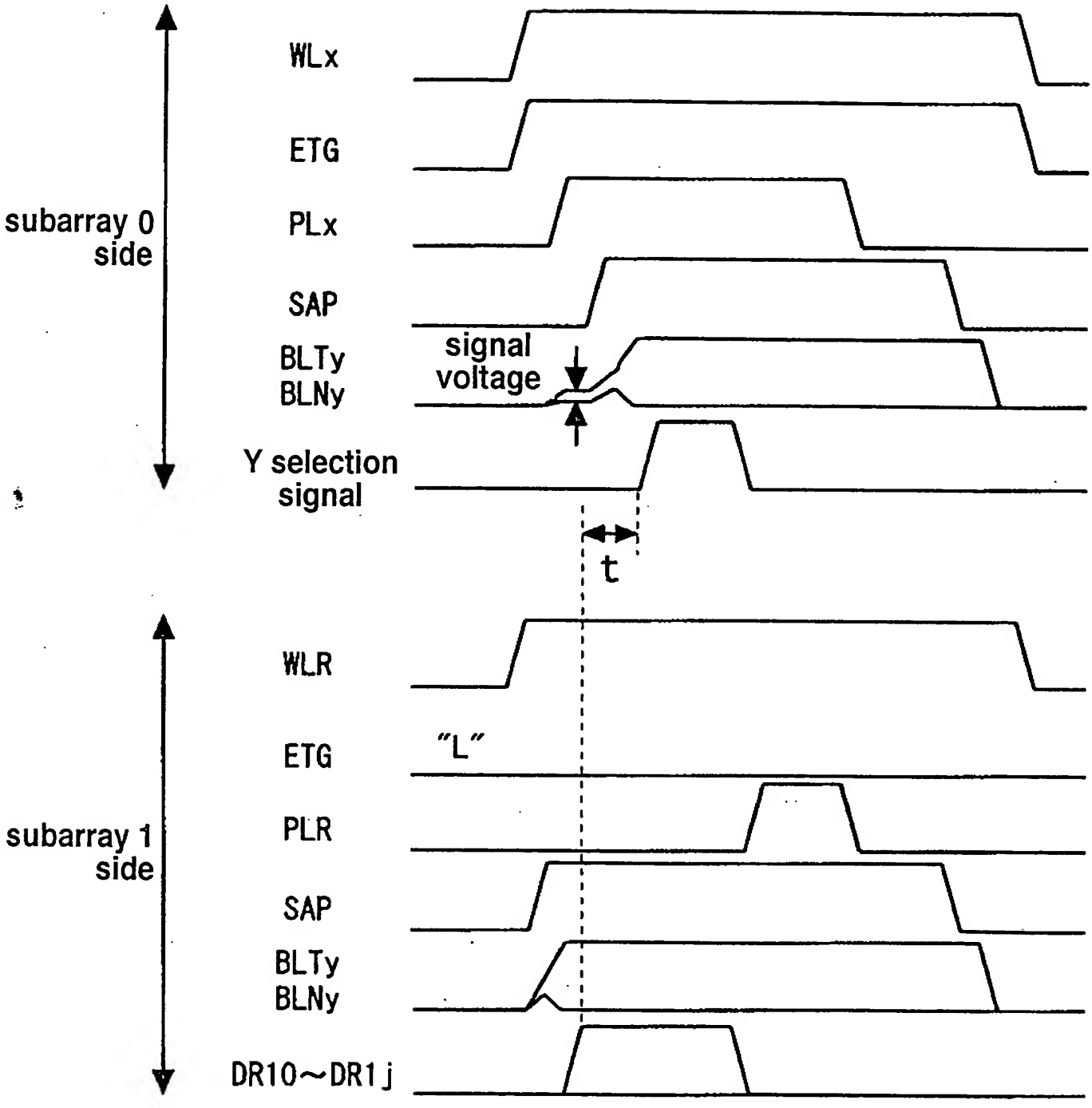

subarray 0 side
WLx
ETG
PLx
SAP
BLTy
BLNy
signal voltage
Y selection signal
t
subarray 1 side
WLR
ETG
"L"
PLR
SAP
BLTy
BLNy
DR10~DR1j

Fig. 13

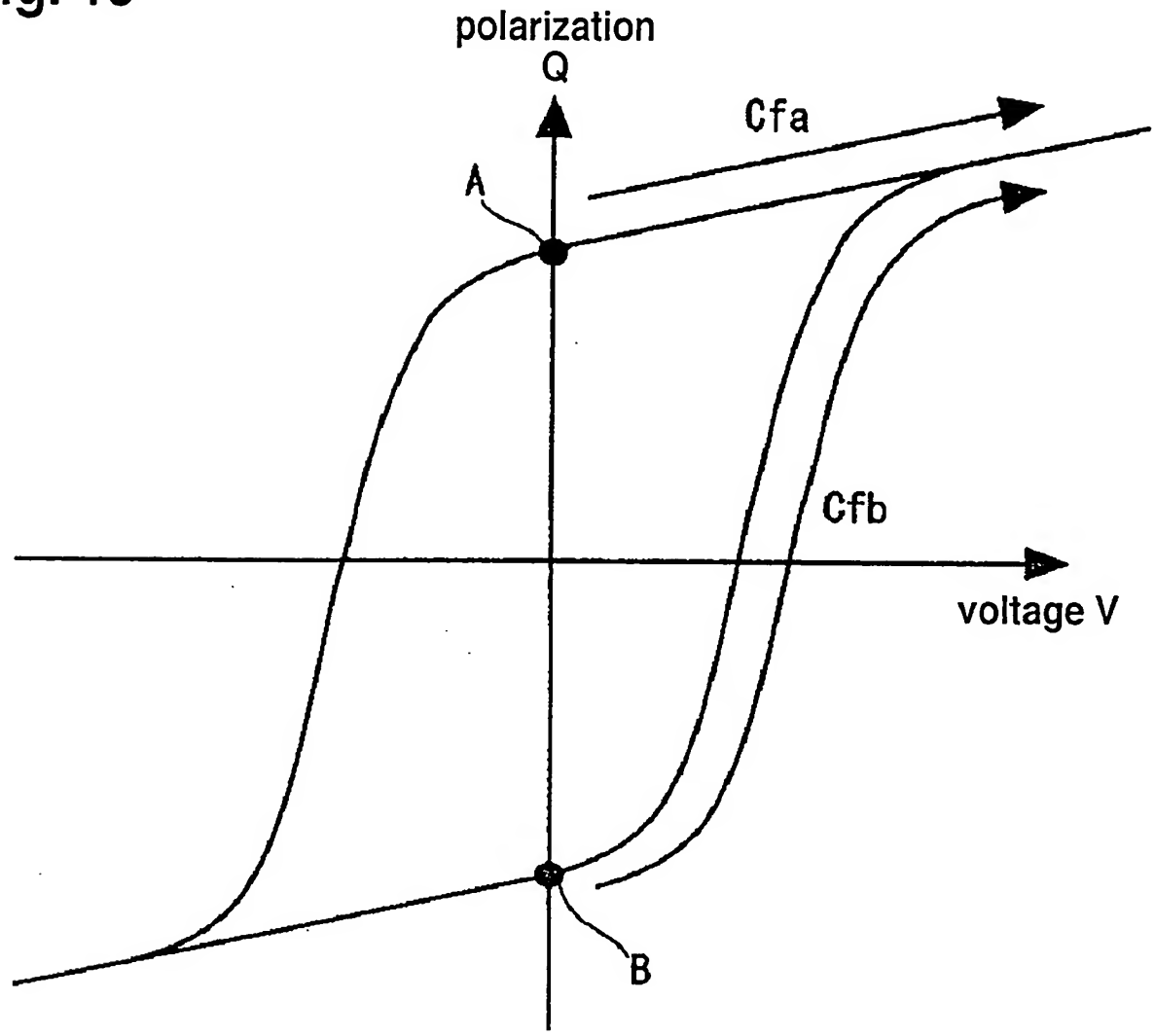


Fig. 14

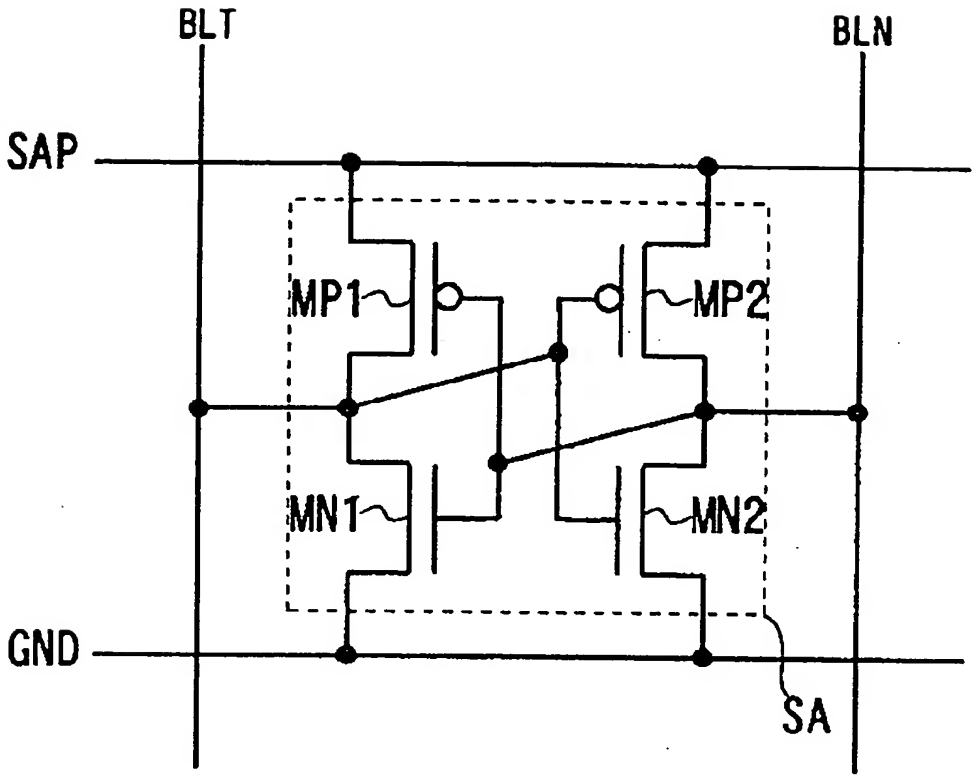


Fig. 15

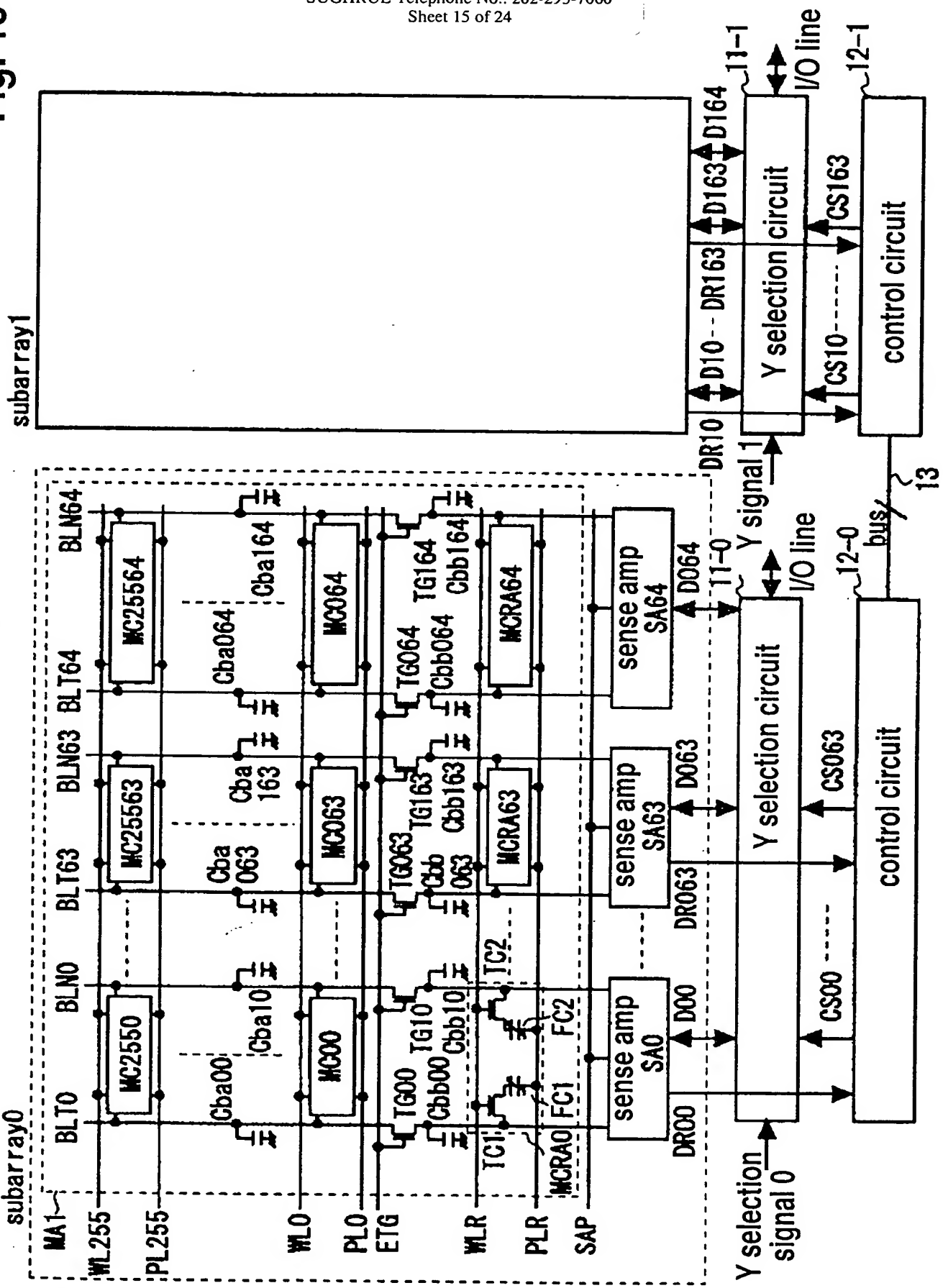

subarray1
subarray0
MA1
WL255
PL255
BLT0
BLN0
BLT63
BLN63
BLT64
BLN64
MC2550
MC25563
MC25564
Cba00
Cba10
Cba063
Cba163
Cba064
Cba164
WL0
PL0
ETG
MC000
MC063
MC064
TG000
TG010
TG063
TG163
TG064
TG164
Cbb00
Cbb10
Cbb063
Cbb163
Cbb064
Cbb164
WLR
PLR
SAP
TC1
TC2
FC1
FC2
MCRA0
MCRA63
MCRA64
sense amp SA0
sense amp SA63
sense amp SA64
DR00
DR063
DR10
DO0
DO63
DO64
DR10 - DR163
D10 - D164
11-0
11-1
Y selection circuit
Y signal 1
Y selection signal 0
I/O line
12-0
12-1
CS00
CS063
CS10
CS163
control circuit
bus
13

Fig. 16

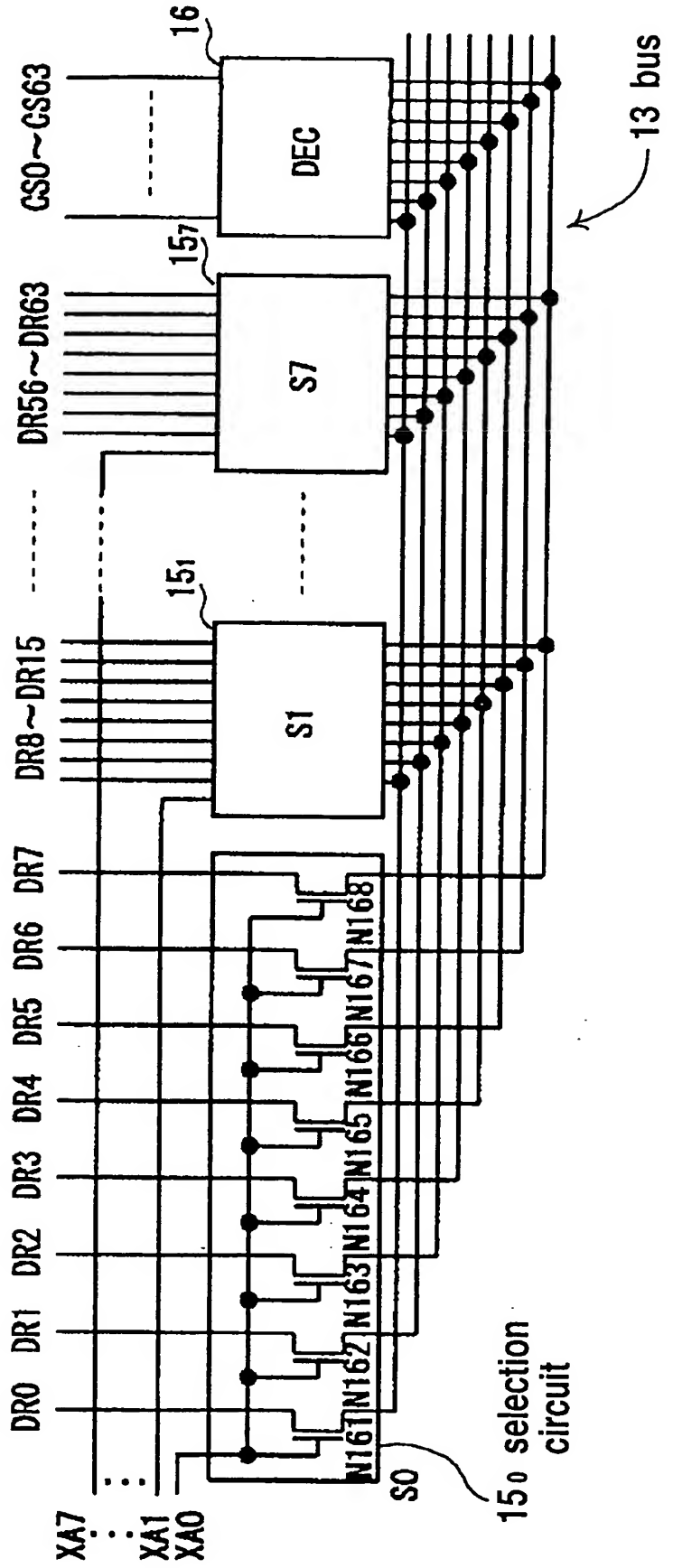

16
CS0~CS63
DEC
13 bus
157
DR56~DR63
S7
151
DR8~DR15
S1
DR7
DR6
DR5
DR4
DR3
DR2
DR1
DR0
N168
N167
N166
N165
N164
N163
N162
N161
S0
150 selection circuit
XA7
XA1
XA0

Fig. 17

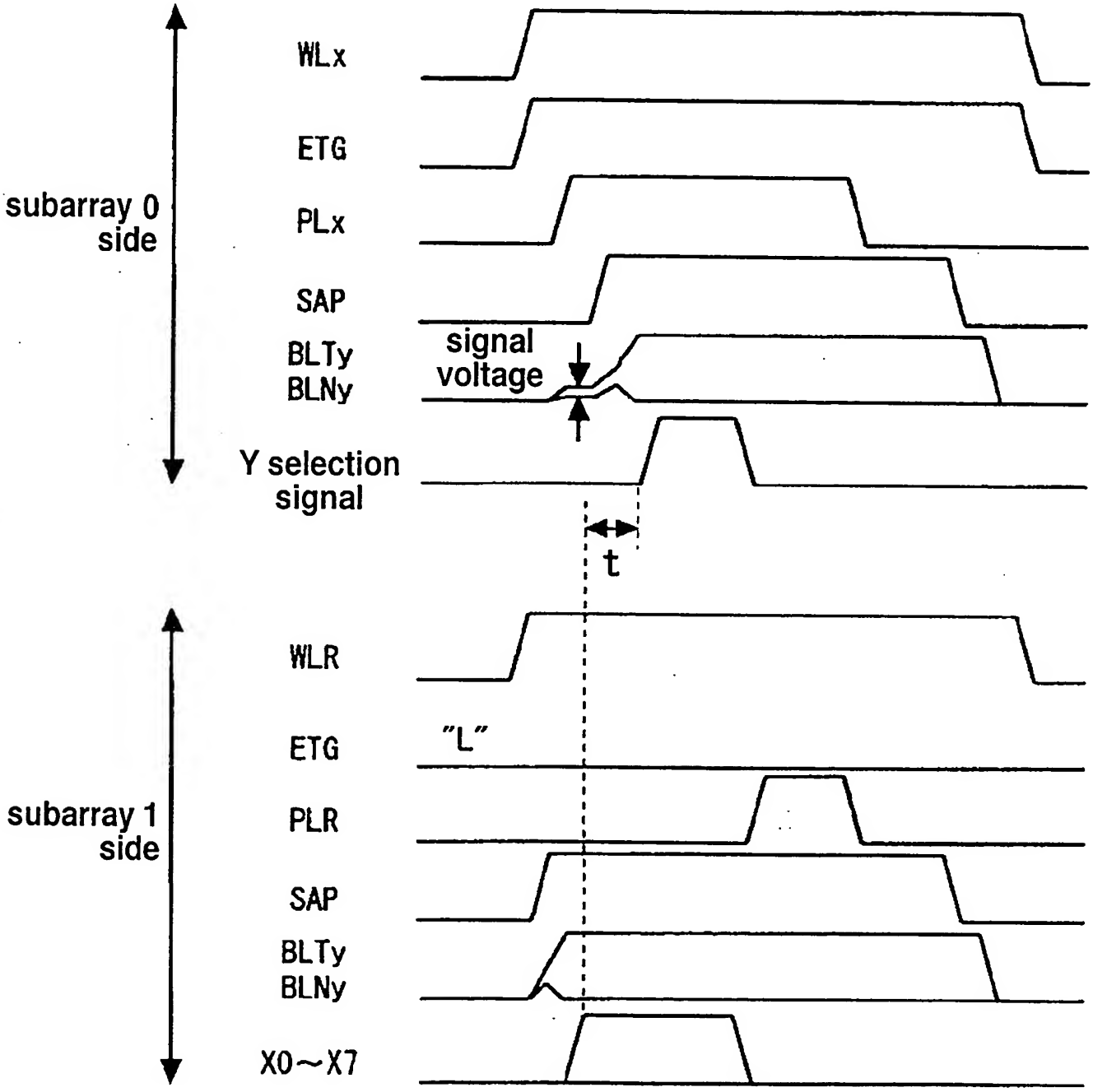

subarray 0 side
WLx
ETG
PLx
SAP
BLTy
BLNy
signal voltage
Y selection signal
t
subarray 1 side
WLR
ETG
"L"
PLR
SAP
BLTy
BLNy
X0~X7

Fig. 18

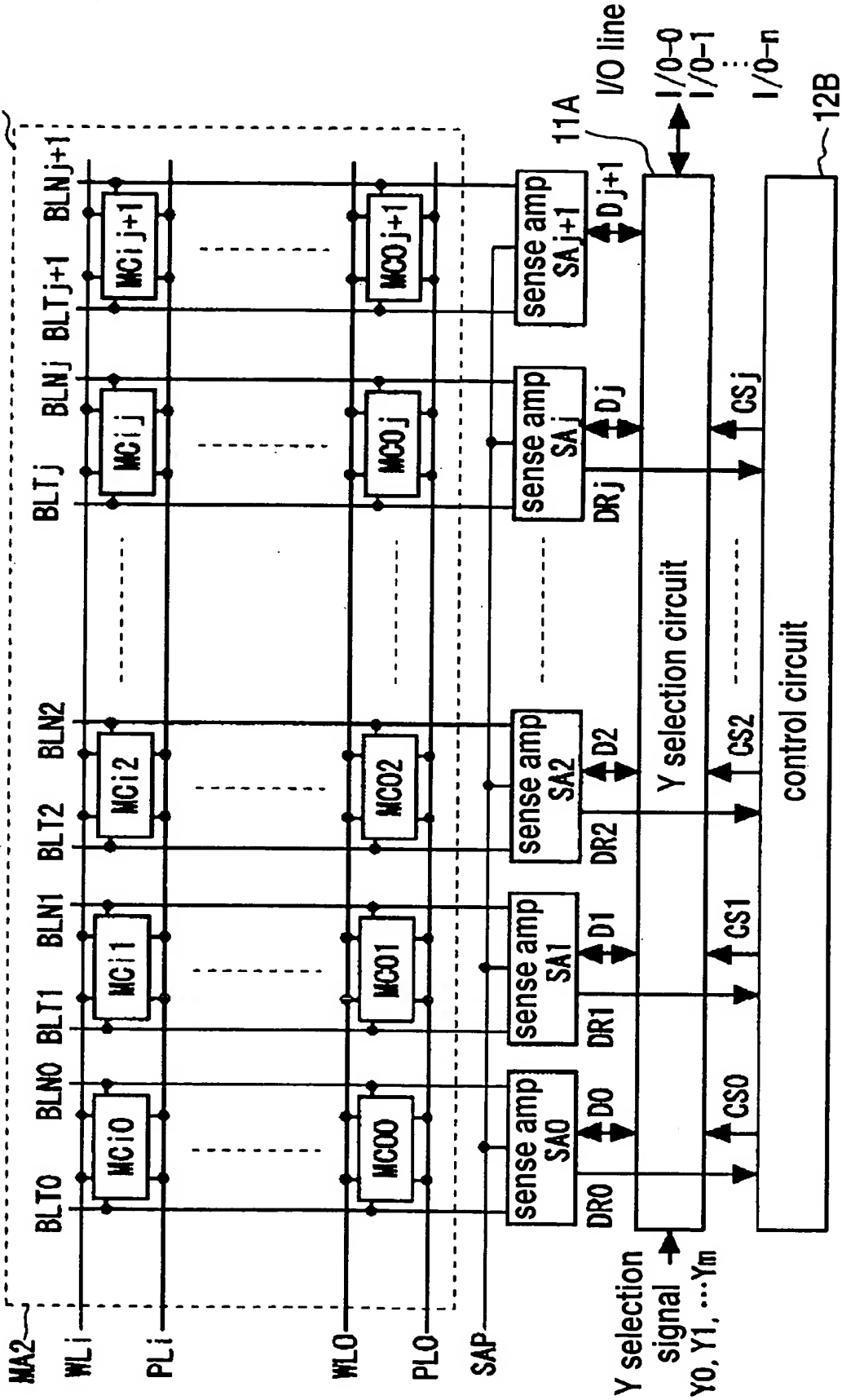

10
11A
12B
I/O line
I/O-0
I/O-1
I/O-n
BLNj+1
BLTj+1
BLNj
BLTj
BLN2
BLT2
BLN1
BLT1
BLN0
BLT0
MCij+1
MCOj+1
MCij
MCOj
MCi2
MCO2
MCi1
MCO1
MCi0
MCO0
sense amp SAj+1
sense amp SAj
sense amp SA2
sense amp SA1
sense amp SA0
Dj+1
Dj
D2
D1
D0
DRj
DR2
DR1
DR0
CSj
CS2
CS1
CS0
Y selection circuit
control circuit
MA2
WLi
PLi
WLO
PLO
SAP
Y selection signal
Y0, Y1, ...Ym

Fig. 19

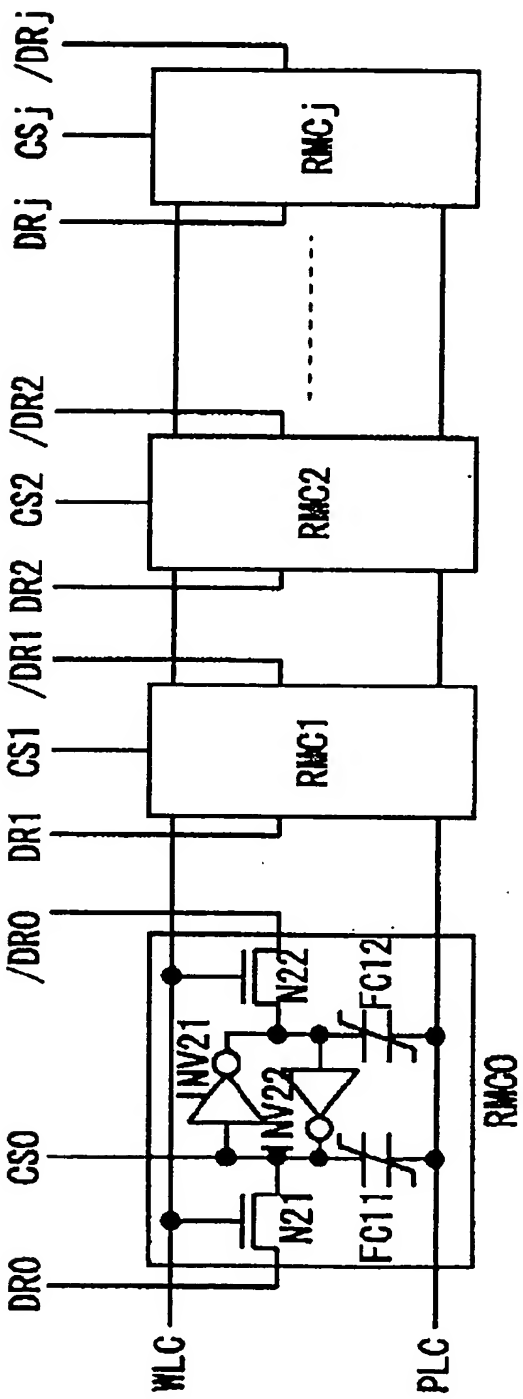

/DRj
CSj
DRj
RMCj
/DR2
CS2
DR2
RMC2
/DR1
CS1
DR1
RMC1
/DR0
CS0
DR0
N22
FC12
INV21
INV22
N21
FC11
RMC0
WLC
PLC

Fig. 20

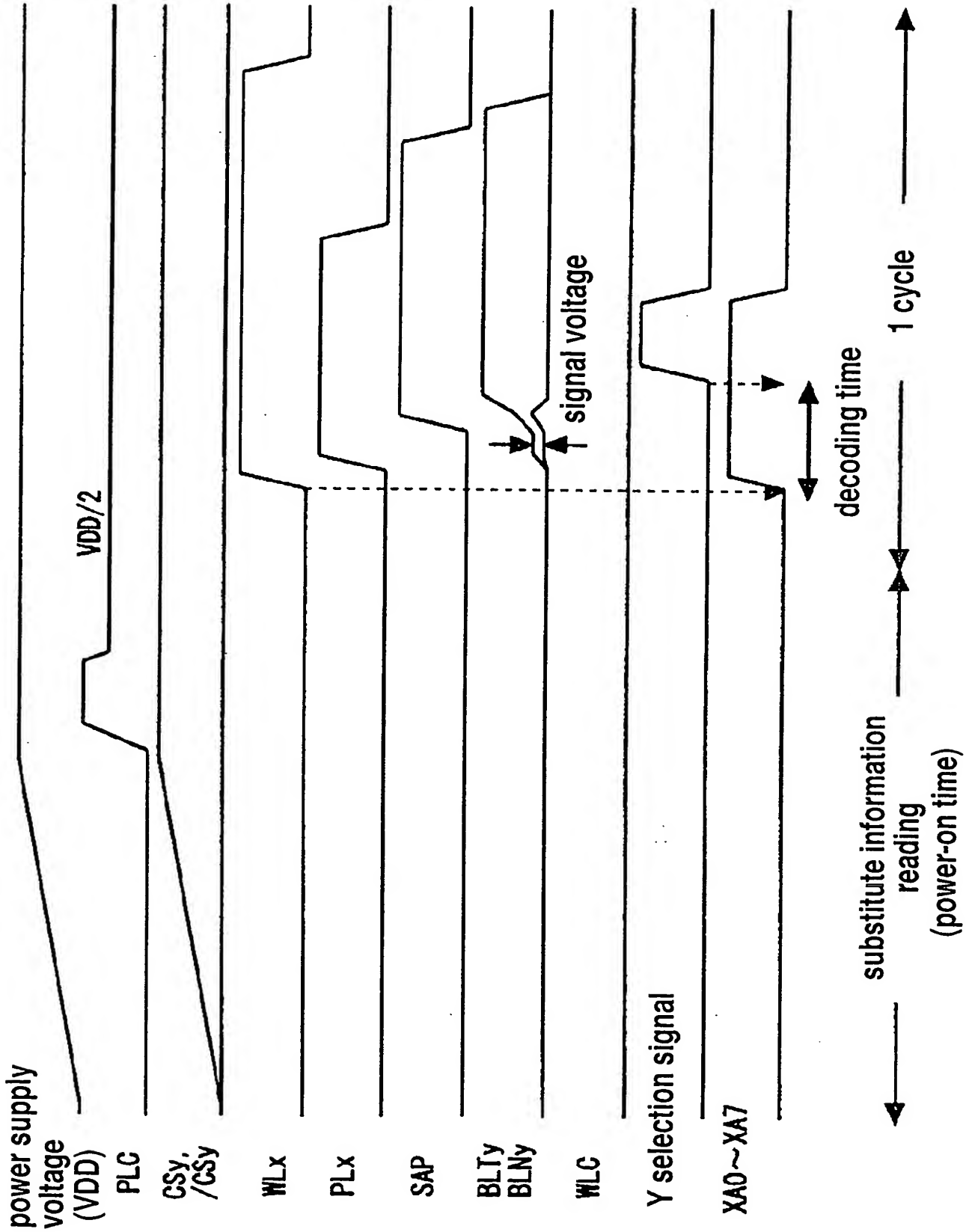

power supply voltage (VDD)
VDD/2
PLC
CSy, /CSy
WLx
PLx
SAP
BLTy BLNy
WLC
Y selection signal
XA0~XA7
signal voltage
decoding time
1 cycle
substitute information reading (power-on time)

Fig. 21

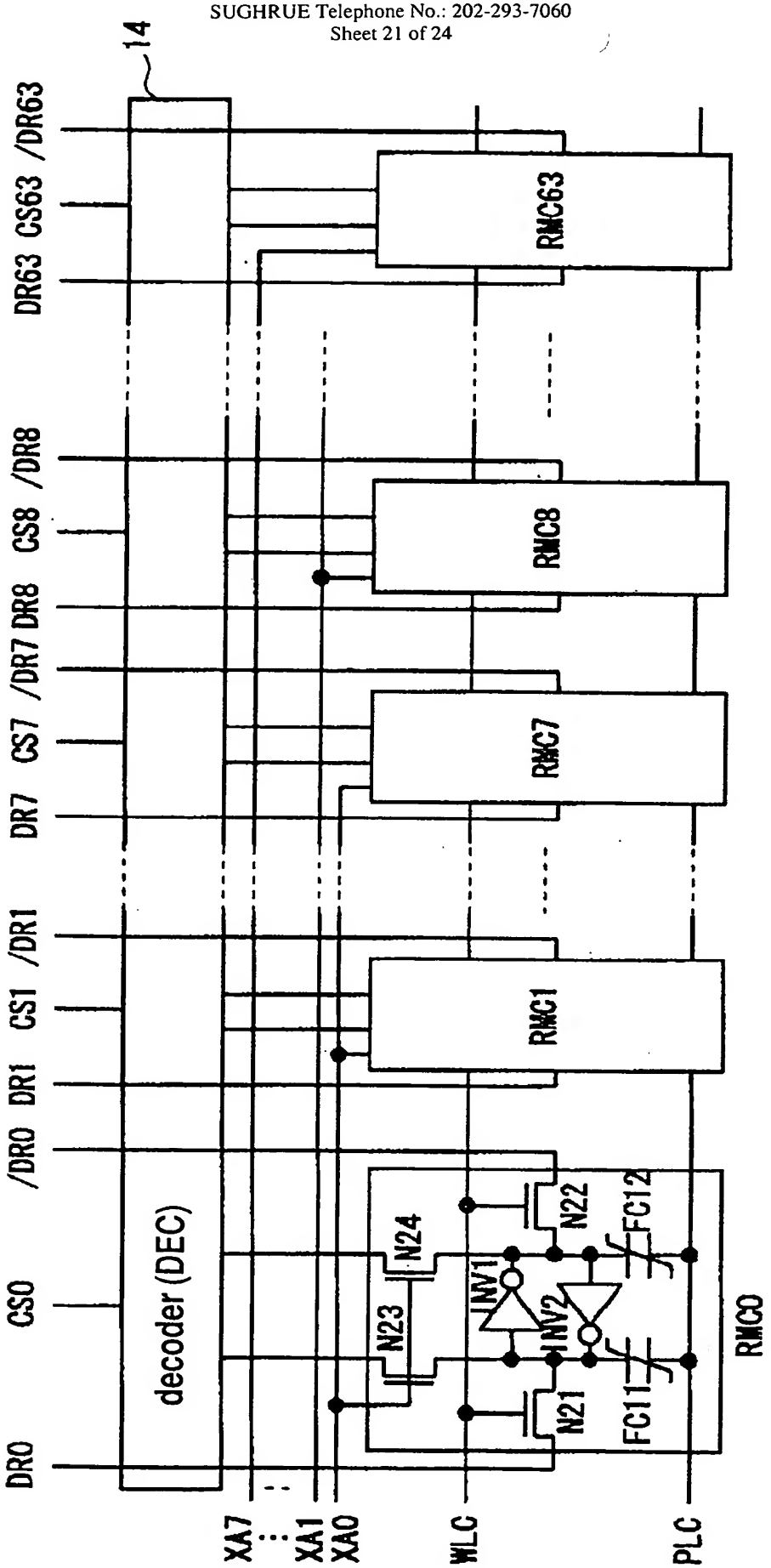
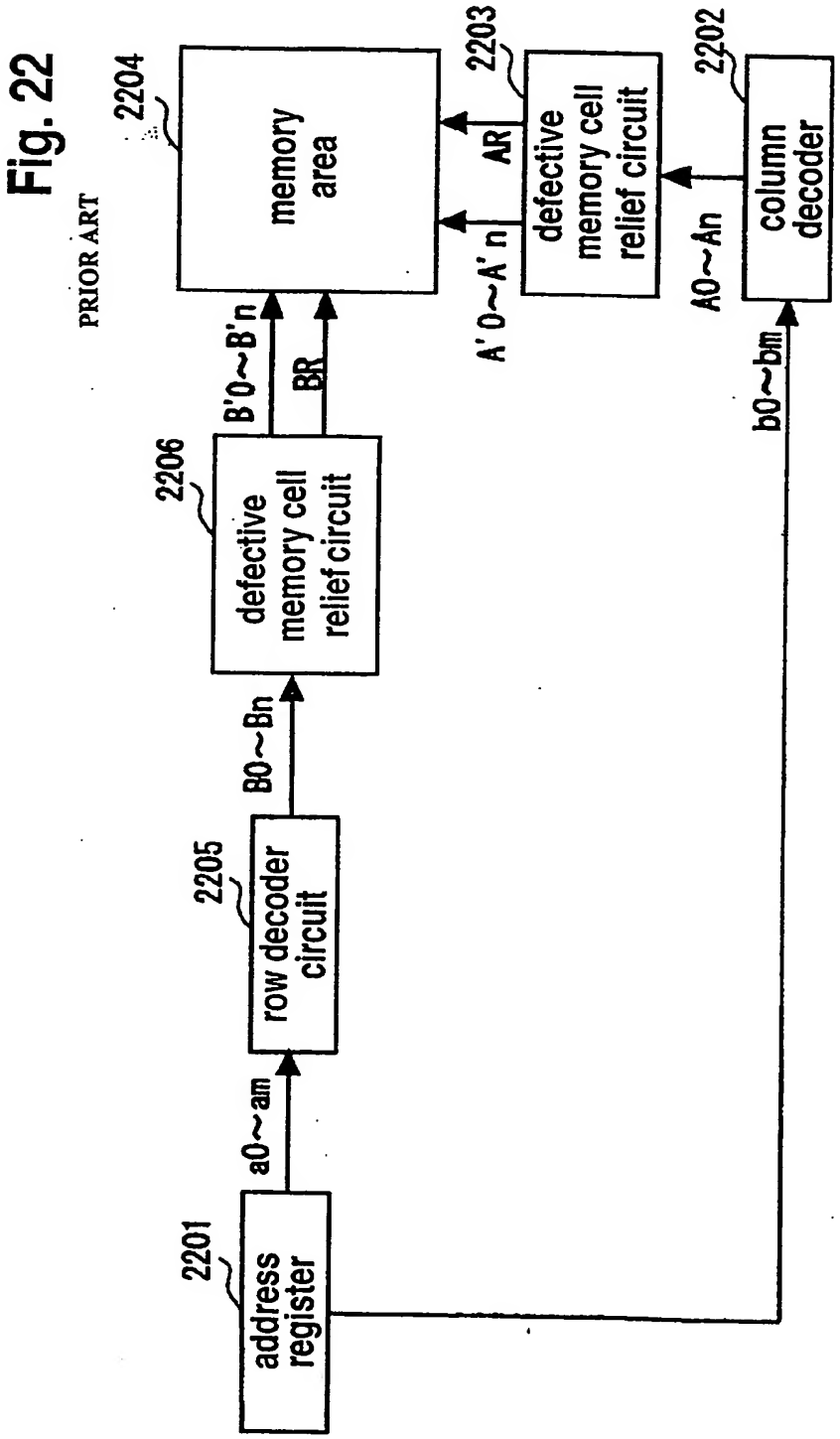

14
DR63
CS63
/DR63
DR8
CS8
/DR8
DR7
CS7
/DR7
DR1
CS1
/DR1
DR0
CS0
/DR0
RMC63
RMC8
RMC7
RMC1
RMC0
decoder (DEC)
N22
FC12
N24
INV1
INV2
N23
N21
FC11
XA7
XA1
XA0
WLC
PLC

Fig. 22
PRIOR ART



PRIOR ART

Fig. 23

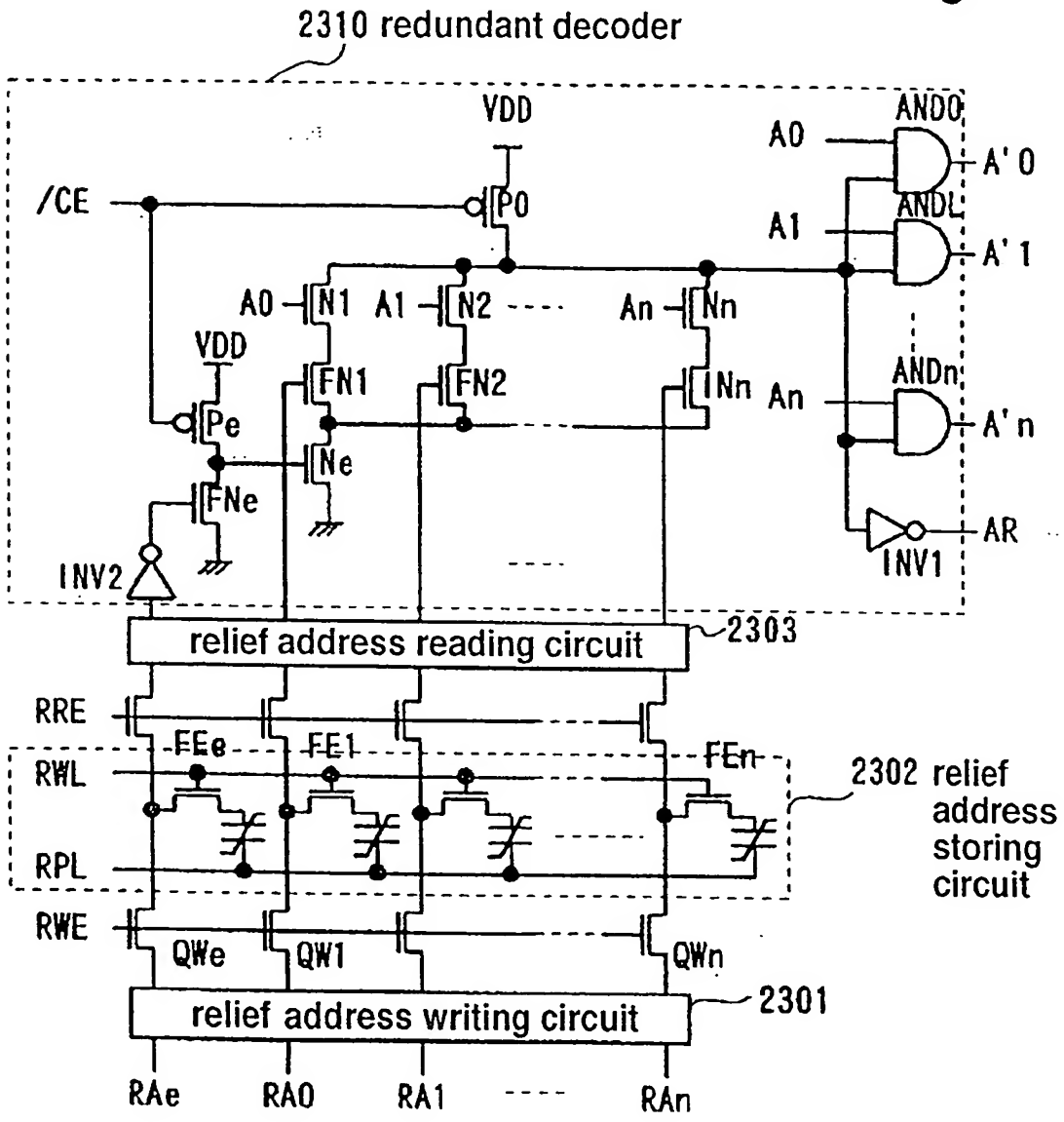


Fig. 24

PRIOR ART